is calibrated so as to terminate inside a heavily doped region (the edge portion **4***b* of the first doped region **4**), which represents a guard region against the concentrations of electrical field. The same heavily doped region connects an active region of the power device (for example an anode region in the case of the diode, or else a body region in the case of the MOSFET) with a ring region of the edge-termination structure. The resulting structure is consequently extremely efficient and enables prevention of breakdown phenomena of the power device (which can have a cut-off voltage that can even reach 1500 V, according to the thickness of the epitaxial layer).

[0055] Finally, it is clear that modifications and variations can be made to what is described and illustrated herein, without thereby departing from the scope of the present invention.

[0056] In particular, it is clear that, applying the concepts described, it is possible to obtain different power devices, for example an IGBT (insulated-gate bipolar transistor), a BJT, or a Schottky diode.

[0057] Furthermore, the possibility of obtaining dual structures, in which the charge balance is achieved by means of formation of N-doped columnar structures in a P-doped epitaxial layer is evident.

[0058] The columnar structures **7** may extend throughout the thickness of the epitaxial layer **3**, terminating inside the substrate **2**. As further alternative, a buffer layer, for example of an N type, can be provided between the substrate **2** and the epitaxial layer **3**, and the columnar structures **7** may terminate in the buffer layer.

[0059] Furthermore, the concepts underlying the described process may be applied in a generic power device, in which it is provided, on the top surface of the wafer, a doped surface layer extending also in the edge area, envisaging etching and removal of said layer at the edge area, stopping the etching inside a heavily doped guard region, in order to limit breakdown phenomena.

[0060] A device formed according to an above-described process or otherwise having the above-described structure may be part of a circuit, such as a power supply, and the circuit may be part of a system, such as a computer system.

[0061] From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention.

1. A process for manufacturing a semiconductor power device, comprising:

providing a body made of semiconductor material having a first top surface;

forming an active region with a first type of conductivity in the proximity of said first top surface and inside an active portion of said body; and

forming an edge-termination structure, comprising a ring region having said first type of conductivity and a first doping level, set within a peripheral edge portion of said body and electrically connected to said active region,

wherein said step of forming an edge-termination structure further comprises forming a guard region, having said first type of conductivity and a second doping level, higher than said first doping level, in the proximity of said first top surface and connecting said active region to said ring region; and in that it further comprises:

forming a surface layer having said first type of conductivity on said first top surface, also at said peripheral edge portion, in contact with said guard region; and

etching said surface layer in order to remove it above said edge portion in such a manner that the etch terminates inside said guard region.

2. The process according to claim **1**, wherein said step of etching said surface layer further comprises etching a surface portion of said body in such a manner that said body has, at said peripheral edge portion, a second top surface set at a lower level with respect to said first top surface, and that a step is thus formed inside said guard region, connecting said first and second top surfaces.

3. The process according to claim **2**, wherein said step of etching a surface portion of said body (**3**) comprises planarizing said second top surface (**3***b*).

4. The process according to claim **2**, wherein forming said active region comprises arranging said active region in such a manner that it extends as far as a first level, at least corresponding to said first top surface, and forming said ring region comprises arranging said ring region in such a manner that it extends as far as a second level, lower than said first level and corresponding to said second top surface.

5. The process according to claim **4**, wherein arranging said ring region comprises: introducing dopant species of said second type of conductivity inside said body at a distance of separation from said first top surface, prior to said step of etching said surface layer; and causing a process of displacement of said ring region as far as said second top surface after said step of etching said surface layer.

6. The process according to claim **5**, further comprising the steps of growing a thermal-oxide layer above said body after said step of etching said surface layer, and removing said thermal-oxide layer above said active portion; said step of growing a thermal-oxide layer comprising said step of causing a process of displacement of said ring region.

7. The process according to claim **1**, wherein said body has a second type of conductivity, opposite to said first type of conductivity; further comprising the step of forming charge-balance columnar regions having said first type of conductivity through said body, both in said active portion and in said edge portion, and in particular through said guard region and said ring region; said step of forming columnar regions further comprising forming said surface layer and in particular surface extensions of said columnar regions on said first top surface and connection portions between said surface extensions.

8. The process according to claim **7**, wherein said surface layer has a non-planar profile, and said surface extensions have a grooved, in particular substantially V-shaped, surface profile.

9. The process according to claim **7**, wherein forming columnar regions comprises:

forming deep trenches inside said body; and

filling said deep trenches with semiconductor material via non-selective epitaxial growth so as to form said columnar regions inside said deep trenches and said surface extensions on said first top surface; said columnar regions having a doping level such as to substantially balance an opposite doping level of said body.

10. The process according to claim **9**, wherein filling said deep trenches comprises supplying a gas containing said semiconductor material and a gas containing dopant ions of